

MOS FIELD EFFECT TRANSISTOR

2SK3354

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK3354 is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super low on-state resistance:
- ★ RDS(on)1 = 8.0 m Ω MAX. (VGS = 10 V, ID = 42 A)
- ★ RDS(on)2 = $12 \text{ m}\Omega$ MAX. (Vgs = 4 V, ID = 42 A)
- ★ Low Ciss: Ciss = 6300 pF TYP.
 - Built-in gate protection diode

ORDERING INFORMATION

PART NUMBER	PACKAGE		
2SK3354	TO-220AB		
2SK3354-S	TO-262		
2SK3354-Z	TO-220SMD		

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

	Drain to Source Voltage	V _{DSS}	60	V
	Gate to Source Voltage	VGSS(AC)	±20	V
	Drain Current (DC)	I _{D(DC)}	±83	Α
	Drain Current (pulse) Note1	D(pulse)	±332	Α
	Total Power Dissipation (Tc = 25°C)	PT	100	W
	Total Power Dissipation (T _A = 25°C)	PT	1.5	W
	Channel Temperature	Tch	150	°C
	Storage Temperature	T_{stg}	-55 to +150	°C
*	Single Avalanche Current Note2	las	55	Α
*	Single Avalanche Energy Note2	Eas	302	mJ

Notes 1. PW \leq 10 μ s, Duty cycle \leq 1 %

2. Starting Tch = 25 °C, RG = 25 Ω , VGs = 20 V \rightarrow 0 V

THERMAL RESISTANCE

Channel to Case	Rth(ch-C)	1.25	°C/W
Channel to Ambient	Rth(ch-A)	83.3	°C/W

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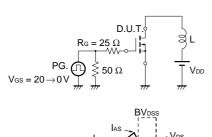
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.



* ELECTRICAL CHARACTERISTICS (TA = 25 °C)

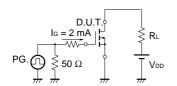
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, ID = 42 A		6.3	8.0	mΩ
	RDS(on)2	Vgs = 4 V, ID = 42 A		8.0	12	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 42 A	35	59		S
Drain Leakage Current	IDSS	Vps = 60 V, Vgs = 0 V			10	μΑ
Gate to Source Leakage Current	lgss	Vgs = ±20 V, Vps = 0 V			±10	μΑ
Input Capacitance	Ciss	Vps = 10 V, Vgs = 0 V, f = 1 MHz		6300		pF
Output Capacitance	Coss			1000		pF
Reverse Transfer Capacitance	Crss			490		pF
Turn-on Delay Time	td(on)	$I_D = 42 \text{ A}, V_{GS(on)} = 10 \text{ V}, V_{DD} = 30 \text{ V},$		100		ns
Rise Time	tr	$R_G = 10 \Omega$		1500		ns
Turn-off Delay Time	t _{d(off)}			300		ns
Fall Time	tf			440		ns
Total Gate Charge	Q _G	ID = 83 A , VDD = 48 V, VGS = 10 V		106		nC
Gate to Source Charge	Qgs			20		nC
Gate to Drain Charge	Q _{GD}			30		nC
Body Diode Forward Voltage	VF(S-D)	IF = 83 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 83 A, VGS = 0 V,		55		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		100		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

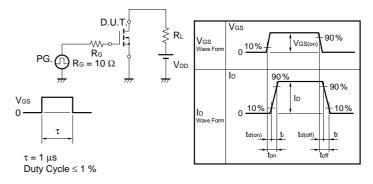


-Starting Tch

TEST CIRCUIT 3 GATE CHARGE



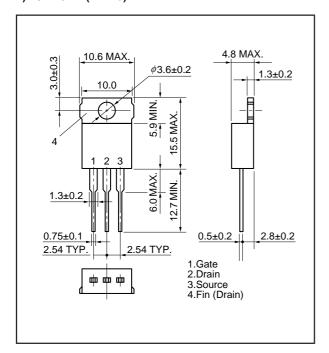
TEST CIRCUIT 2 SWITCHING TIME



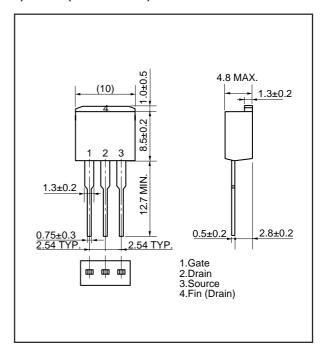


PACKAGE DRAWING (Unit: mm)

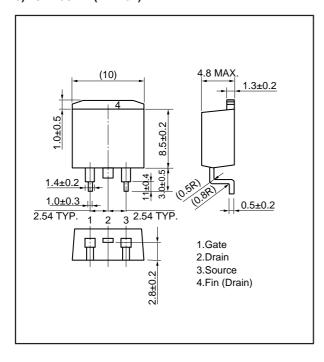
1) TO-220AB (MP-25)



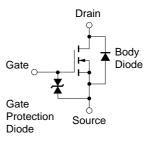
2) TO-262 (MP-25 Fin Cut)



3) TO-220SMD (MP-25Z)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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